

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an input terminal to receive an external voltage;

and

a voltage formation circuit to provide an internal voltage based on said external voltage,

wherein said internal voltage has a first change rate in accordance with a change of said external voltage, when said external voltage is in a first voltage range,

wherein said internal voltage has a second change rate in accordance with the change of said external voltage, when said external voltage is in a second voltage range, said second change rate being different from said first change rate, and

wherein said second voltage range is larger than said first voltage range.

2. A semiconductor device according to claim 1,

wherein said internal voltage has a third change rate in accordance with the change of said external voltage, when said external voltage is in a third voltage range, said third change rate being different from said second change rate, and

wherein said third voltage range is larger than said second voltage range.

3. A semiconductor device according to claim 2,
wherein said first voltage range and said second
voltage range are successive ranges, and
wherein said second voltage range and said third
voltage range are successive ranges.

4. A semiconductor device according to claim 2,
wherein said external voltage of said second voltage
range is applied in a normal operation of said semiconductor
device, and
wherein said external voltage of said third voltage
range is applied in a test operation of said semiconductor
device.

5. A semiconductor device according to claim 4,
wherein said test operation is a burn-in test
operation.

6. A semiconductor device according to claim 2,
wherein said second change rate is substantially 0.

7. A semiconductor device according to claim 2,
wherein said first change rate is different from
said third change rate.

8. A semiconductor device according to claim 2,
wherein said first change rate is the same as said
third change rate.

9. A semiconductor device according to claim 2,
wherein said internal voltage is applied to a P type
well region of a semiconductor substrate of said semiconductor
device.

10. A semiconductor device comprising:
an input terminal to receive an external voltage;
and
a voltage generation circuit to provide an internal
voltage based on said external voltage, said internal voltage
being a negative voltage,
wherein the absolute value of a change of said
internal voltage in accordance with a change of said external
voltage is a first value, when said external voltage is in a
first voltage range,
wherein the absolute value of the change of said
internal voltage in accordance with the change of said
external voltage is a second value, when said external voltage
is in a second voltage range, said second value being smaller
than said first value,
wherein the absolute value of the change of said
internal voltage in accordance with the change of said

external voltage is a third value, when said external voltage is in a third voltage range, said third value being larger than said second value,

wherein said second voltage range is larger than said first voltage range, and

wherein said third voltage range is larger than said second voltage range.

11. A semiconductor device according to claim 10,
wherein said first voltage range and said second voltage range are successive ranges, and

wherein said second voltage range and said third voltage range are successive ranges.

12. A semiconductor device according to claim 10,
wherein said external voltage of said second voltage range is applied in a normal operation of said semiconductor device, and

wherein said external voltage of said third voltage range is applied in a test operation of said semiconductor device.

13. A semiconductor device according to claim 12,
wherein said test operation is a burn-in test operation.

14. A semiconductor device according to claim 10,
wherein said second value is substantially 0.

15. A semiconductor device according to claim 10,
wherein said first change rate is different from
said third change rate.

16. A semiconductor device according to claim 10,
wherein said first change rate is the same as said
third change rate.

17. A semiconductor device according to claim 10,
wherein said internal voltage is applied to a P type
well region of a semiconductor substrate of said semiconductor
device.

18. A semiconductor device comprising a voltage forming
circuit to provide a first voltage,
wherein said first voltage is a negative voltage,
wherein said first voltage is a stable voltage when
said semiconductor device is in a normal operation, and
wherein said first voltage changes in accordance
with an external power supply voltage when said semiconductor
device is in a test operation.

19. A semiconductor device according to claim 18,
wherein said test operation is a burn-in test
operation.

20. A semiconductor device according to claim 19,
wherein said first voltage is applied to a P type
well region formed in a semiconductor substrate of said
semiconductor device.

21. A semiconductor device comprising:
an input terminal to receive an external voltage;
and
a voltage generation circuit to provide an internal
voltage in accordance with said external voltage, said
internal voltage being a negative voltage,
wherein the absolute value of the change of said
internal voltage in accordance with a change of said external
voltage is a first value, when said external voltage is in a
first voltage range,
wherein the absolute value of the change of said
internal voltage in accordance with the change of said
external voltage is a second value, when said external voltage
is in a second voltage range, said second value being larger
than said first value,
wherein said second voltage range is larger than
said first voltage range, and

wherein said external voltage of said first voltage range is applied in a normal operation of said semiconductor device.

22. A semiconductor device according to claim 21, wherein said first voltage range and said second voltage range are successive ranges.

23. A semiconductor device according to claim 21, wherein said external voltage of said second voltage range is applied in a burn-in test operation of said semiconductor device.

24. A semiconductor device according to claim 21, further comprising:

a plurality of memory cells each of which comprises a N-channel transistor having source and drain regions formed in a P type well region,

wherein said internal voltage is applied to said P type well region formed in a semiconductor substrate of said semiconductor device.